

# UBM Electronics | Virtual Event Solutions

Connect, collaborate and drive deeper engagements with design decision makers



**Presented by:** EE Times  
**Live Date:** Thursday, May 12, 2011, 11amET – 6pmET  
**On-Demand:** May 13, 2011 – November 13, 2011  
**URL:** <http://vc.ubmelectronics/soc> (live 3/31)  
**Conference Co-Chairs:** Mike Demler, Technical Editor, EDN Magazine  
 Clive "Max" Maxfield, President, Maxfield High-Tech Consulting

## Not Your Mother's SoC: Combining IP Reuse with HLS in an Integrated SoC Design and Verification Flow

One of the great productivity boosters in SoC design today is the use of High-Level Synthesis (HLS), which has equally beneficial impacts in both the design and verification flows. HLS increases productivity and reduces risk by allowing users to raise the level of design abstraction, to explore a greater range of "what-if" architectural scenarios, and to more fully analyze and verify the high-level functionality of the design before committing to a final implementation.

Another great productivity booster is the reuse of internally-generated and third-party-provided silicon intellectual property (IP). The use of IP has been growing steadily over the years. Depending on the design in question, IP blocks may account for anywhere up to 90% of the design.

But can an IP reuse methodology work within a high-level synthesis flow? Our virtual conference will explore how the industry's top design and verifications teams are approaching the problem.

### Who Should Participate

- **Building an SoC Flow Optimized for IP Integration**  
Companies that develop: IP models, tools to link high-level models together, tools to define and implement on-chip interconnect topologies (busses, networks)...
- **Applying High-Level Synthesis in an SoC Flow**  
Companies that develop: Modeling solutions, Verification solutions, High-Level Synthesis solutions...
- **Hardware/Software Co-Design, Co-Verification, and Integration**  
Companies and users who have real world experiences designing and verifying SoCs using today's tools, technologies, and flows; also those who are driving the next-generation of tools, technologies, and flows...

### Why Virtual Events?

Attendees of EE Times Virtual Conferences learn from and interact directly with industry experts and technology providers via keynote speeches, webinars, moderated discussion panels, and live interactive chats, and gain access to a comprehensive collection of educational material and resources on the topic.

### Sponsor Benefits

Reach your target audience through a highly interactive platform and receive:

- Targeted, global access to focused design decision makers
  - Alignment with award winning editorial content
  - Attendee tracking and reporting
  - Advanced platform to promote your rich media assets
  - Immediate interaction with customers and prospects
- Targeted leads with detailed demographic data.

### About UBM Electronics

UBM Electronics, a UBM company, is the global leader in media and marketing services for the electronics industry. Each month more than 2.2 million global electronics industry professionals engage with our online, event and print brands and communities. We serve marketers with targeted, deep and measurable engagement with our audience, and we offer innovative, nextgen marketing services built around industry-leading editorial content.

# UBM Electronics | Virtual Event Solutions

Connect, collaborate and drive deeper engagements with design decision makers

## Who Will Participate

- IP Developers
- System Architects
- DSP Designers
- Hardware Design Engineers
- Embedded Software and Firmware Developers
- Verification Engineers
- Project Managers

## About the Technical Program

A combination of sponsored and editorially selected panelists will participate in the sessions listed below. Additional sessions in the program include a keynote address and one or more sponsored webinars.

### Panel Discussion: Building an SoC Flow Optimized for IP Integration

A digital IP block is not just a piece of hardware described at the RT level anymore; it is a complex interaction of functionality described in both the hardware and software domains. Many models are required for the hardware – often at multiple levels of abstraction, along with hardware and software interfaces, the ways in which the block can be integrated into a system, the verification environment, and much, much more. The lack of standards to define all of the necessary models and abstractions means that making everything work together can be a veritable nightmare. And we also have to consider hard IP blocks and analog/mixed-signal IP. What can be done to help bring about some sanity into this flow?

### Panel Discussion: Applying High-Level Synthesis (HLS) in an SoC Flow

While integration of IP blocks can ease the process of building an SoC, every chip needs new or unique capabilities and the complexity of these customized portions of the design is rising. RTL has become unwieldy at handling the size and complexity associated with designing the right architecture and then implementing and verifying this architecture. High-level synthesis technologies are emerging as a solution in this area, but can they solve all of your problems and how do they integrate into the rest of the IP-based system?

### Panel Discussion: Hardware/Software Co-Design, Co-Verification, and Integration

Today's SoCs development teams are no longer focused only on hardware. Embedded software, firmware, drivers, middleware, and applications have recently taken over the spotlight and require a holistic systems approach. Although today's high-level synthesis technologies are currently focused on hardware, similar technologies for use in the software domain are on the horizon. Similarly, the term IP no longer refers only to digital design blocks specified in RTL. Today's IP includes hardware and software; analog, digital, and mixed-signal; and design and verification. This track will focus on hardware/software co-design, co-verification, and integration in the context of a modern SoC development environment that includes a mix of HLS, IP, and much, much more...

Sponsorship pricing opportunities on next page ▶

# UBM Electronics | Virtual Event Solutions

Connect, collaborate and drive deeper engagements with design decision makers

## EE Times Virtual Events

	Exclusive platinum sponsorship	Gold [limit 4]	Silver [unlimited]
<b>Branding Elements</b>			
Recognition as exclusive platinum sponsor of event	Yes	N/A	N/A
Logo: registration page and confirmation emails	Yes	Yes	N/A
Logo: Event advertising	~1 million impressions	~1 million impressions	N/A
Logo: Post event materials	Yes	Yes	Yes
Logo: Plaza Greeting	Yes	Yes	N/A
Booth	<ul style="list-style-type: none"> <li>• Preferred central location</li> <li>• 8 tabs, 40 pieces of content</li> <li>• In booth marquee message</li> <li>• 3 clickable custom graphics</li> <li>• 2 clickable marquee message</li> </ul>	<ul style="list-style-type: none"> <li>• 6 tabs, 30 pieces of content</li> <li>• In booth marquee message</li> <li>• 2 clickable custom graphics</li> <li>• 1 clickable marquee message</li> </ul>	<ul style="list-style-type: none"> <li>• 4 tabs, 20 pieces of content</li> <li>• In booth marquee message</li> </ul>
Audience briefcase	2 pieces of content	1 piece of content	N/A
<b>Thought Leadership</b>			
Keynote	30 second promotional video	N/A	N/A
Editorial panel participation	Option to participate in 2 of 3 panels	Option to participate in 1 panel	N/A
Content Pavilion participation	10 pieces of content and co-host invitation	5 pieces of content and co-host invitation	N/A
Attendee interaction: Chat and email	Yes	Yes	Yes
<b>Lead Generation</b>			
Leads: live and archive	Leads from all event registrants, associated booth, webinars, and pavilion areas	Leads from associated booth, webinars, pavilion, and scheduled chat	Booth only
Webinar	<ul style="list-style-type: none"> <li>• 60 minutes live audio</li> <li>• Post session, direct-to-booth</li> </ul>	N/A	N/A
Scheduled Chat	N/A	Yes	N/A
Prize giveaways	Yes	Yes	Yes
Surveys	Yes	Yes	Yes
<b>Price:</b>	\$29,500	\$15,000	\$7,500
A la carte webinar		• 60 minutes live audio	• 60 minutes live audio
<b>Price:</b>	n/a	\$8,000	\$10,000
<b>Recommended Sponsor commitment deadline:</b>	<b>ASAP</b>	6 weeks out from event	3 weeks out from event